Performance Trade-offs and Evolution of ADC Architectures: From Conventional Designs to AI-Driven Hybrid Converters

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Abstract

As the crucial connection between the analog and the digital signal, the analog-to-digital converter (ADC) extremely determine the result of modern electronic systems. It is high performance ADC that essential for advancing emerging technologies, such as wireless communication, medical monitoring and intelligent driving. This article is going to analyze basic principles and key indicators of ADC systematically and respectively, like sampling rate, power consumption and signal-to-noise ratio. It also provides comparative research of four mainstream ADC structures which is called SAR, Flash, Sigma-Delta and Pipeline ADC, evaluating their operating principles and suitable applications. Furthermore, the article investigates hybrid ADC architectures, such as Pipeline-SAR and Flash-SAR ADC, and analyzes modern design trends like dual-channel synchronization through case studies of recent Texas Instruments (TI) products. It is meaningful to mention that future ADC evolution is driving towards innovative materials and architectures, adaptive ability and comprehensive utilization of Artificial Intelligence (AI) three general dimensions. In fact, the combination of advanced nanometer processes, innovative hybrid architectures and AI-based dynamic error correct function are identified as vital ways to achieving higher linearity, lower power consumption and complex environmental auto-adaptation.

Keywords

Analog-to-Digital Converter, Hybrid Architectures, Artificial Intelligence, Performance Optimization.

1. Introduction

In the era of information, electronic systems play a particularly important role in the capture, transmission, and interpretation of information, which is divided into analog signals and digital signals[1][2]. Human perception of the real world, such as light, temperature, and pressure, is essentially a continuous analog signal. In contrast, modern electronic devices, such as microprocessors, use discrete digital signals as medium for high-speed information transmission, but these signals cannot be directly converted to each other. Therefore, the prerequisite for the establishment of all information technology applications is to achieve efficient and accurate conversion from analog to digital signals. An analog-to-digital converter (ADC) is a crucial electronic device used to convert analog signals into digital signals. It is ADC's speed and quality that determines information acquisition and transmission in electronic systems, such as the detection range of radar, the speed of wireless communication or the accuracy of medical devices. So, ADC technology plays a vital role in the advancement of the electronics and information industry. Currently, ADC performance is not only a numerical reference indicator, but also determines the functional boundaries of core technologies and industries. In the field of wireless communication, the ADC is the core of a massive MIMO system. If its performance cannot to reach standards, it will affect communication quality[3-5]. In the medical field, the requirements for ultra-low power consumption and high precision of

ADCs are applied to wearable devices and every interface that need to operate stably and accurately for a long time to monitor patients' physical condition indicators in real time[6][7]. In the field of intelligent driving, high-speed and multi-channel ADCs are the core of sensing devices such as LiDAR and millimeter-wave radar, affecting the accuracy and real-time performance of road condition assessment[8-10]. In conclusion, researching and achieving breakthroughs in high-performance ADCs is a crucial foundation for supporting the future development of information technology[11].

This article focuses on the ADC, an important part of electronic systems, is divided into five parts. The first part is the introduction, which explains the research background and significance. The second part introduces sampling, quantization and encoding as the three basic principles of ADC in converting analog signals to digital signals. It also discusses and analyzes key indicators that determine system performance, such as power consumption, signal-to-noise ratio, effective number of bits, and sampling rate, setting up the theoretical foundation. For the third part, article compares belong four mainstream ADC architectures, including SAR, Flash, Sigma-Delta and Pipeline ADC about their circuit characteristics, performance advantages and disadvantages, and applicable fields. Exploring the current development status of hybrid architecture technology and new ADCs and analyzing the performance improvement brought about by the integration of different architectures is content for the fourth part, moreover, this part uses examples of new products from Texas Instruments (TI), and explores modern design trends such as dual-channel synchronous sampling. As a discussion part, the fifth part, focuses on the development of ADC technology, covering innovative architectures, processes and materials, and cutting-edge applications of artificial intelligence and machine learning in dynamic error correction and adaptive matching. To face the future high-performance and complex environment requirements, what is the development direction of ADC technology

2. Basic Principles and Core Indicators of ADC

2.1. Basic Principles

As a conversion element between the analog and digital domains, the working principle of an ADC includes three main steps which is sampling, quantization and encoding. The sampling circuit samples signals such as voltage, current, or different type of physical quantities from the circuit or environment. Then the samples will go to a quantizer, which maps the sampled voltage values to different digital levels. Finally, the encoder converts the digital signals into binary code for output [12]. However, some ADCs may use Gray or other code due to different encoding methods.

2.2. Core Indicators

2.2.1. Power Consumption

Power consumption means the energy consumed by an ADC during operation, including static and dynamic consumption. Static power consumption mainly includes the small energy consumption by the ADC when it is in standby mode, while dynamic power consumption is the energy consumed by the ADC during operation, such as switching, sampling and conversion.

The power consumption of an ADC is highly related to its design requirements and other factors. For example, ADCs will consume more power when processing high-precision signals. Power consumption generally determines the practicality of an ADC, which is related to its usage, lifespan, and runtime performance. Obviously, power consumption is one of most important indicators of ADC.

2.2.2. Signal to Noise Ratio (SNR)

The signal-to-noise ratio means the ratio of the effective signal power to the noise signal power which is useless, with the unit being decibels (dB). This ratio is usually as shown in equation (2.1).

$$10 \log_{10} \frac{\text{The average power of effective signal}}{\text{The average power of noise signal}} = \text{SNR(dB)} \tag{2.1}$$

From the formula, it is found that as the proportion of effective signal power increases, the higher the signal-to-noise ratio, the better the ADC performance. A low signal-to-noise ratio generally represents that the signal is severely disturbed by the noise signal and easily leads to information distortion. It is all kinds of ADC that have the noise signals after information operation. Ideally, the formula of SNR is as shown in equation (2.2) [13].

$$\text{SNR(dB)} \approx 6.02N + 1.76 \tag{2.2}$$

N in this formula means the number of significant bits. According to the formula, the signal-to-noise ratio of the 10-bit ADC is approximately 61.96dB.

2.2.3. Effective Number of Bits (ENOB)

The effective number of bits means the actual accuracy that an ADC possesses after being affected by various external factors such as noise. According to Formula 2.2, the ENOB can be calculated, as shown in Formula 2.3.

$$\text{ENOB} \approx \frac{\text{SNR(dB)-1.76}}{6.02} \tag{2.3}$$

Ideally, ENOB and SNR is linear correlation. Moreover, a 16 significant bits ADC in theory, but in practical applications, it may only have 13 bits, with the remaining bits being noise and some other useless signals.

2.2.4. Sampling Rate

The sampling rate means the sampling frequency that in a second of the analog input signal, expressed in Hertz (Hz). According to Nyquist's sampling theorem, to completely retain information, the frequency of the sampling signal has to be more than twice as the highest frequency of the input signal, or it may lead to some negative conditions such as distortion which influence the signal. As the formula (2.4) below.

$$f_s \geq 2f_{max} \tag{2.4}$$

The signal will be overlapped if the sampling frequency is too small, in simple, the high-frequency and low-frequency signals are overlapping, resulting in information loss. For example, using an ADC receiver which sampling rate is 10 Hz to sample a cosine wave of 6 Hz, the frequency of Nyquist is half of ADC receiver's which is 5 Hz, less than the frequency of cosine wave and it might be regarded as a 4 Hz signal, that is the information loss.

3. Fundamental ADC Architectures

3.1. SAR ADC

According to the figure 1 that demonstrates how the successive approximation analog-to-digital converter (SAR ADC) work. When the analog signal is input, it first enters the sample-and-hold circuit, and the input voltage will be set as a constant reference value. Then, driven by an external clock, the SAR control logic gradually and successively controls the N-bit DAC, which will output based on the SAR register, generate a reference voltage that gradually approaches the input voltage. Next, comparing the input voltage with the output voltage of the DAC happens in the comparator. If the former is greater than the latter, the comparator outputs "1", otherwise, it outputs "0". These outputs will go to the control logic part, after binary search comparison, those data will be filled in sequence from the highest to the lowest bit. Finally, with the comparation complete, the binary numbers filled in the SAR register are the digital output results. The result is the quantified value of the analog voltage. Almost at the same time, sample-and-hold circuit releases the data and prepares for the next convert.

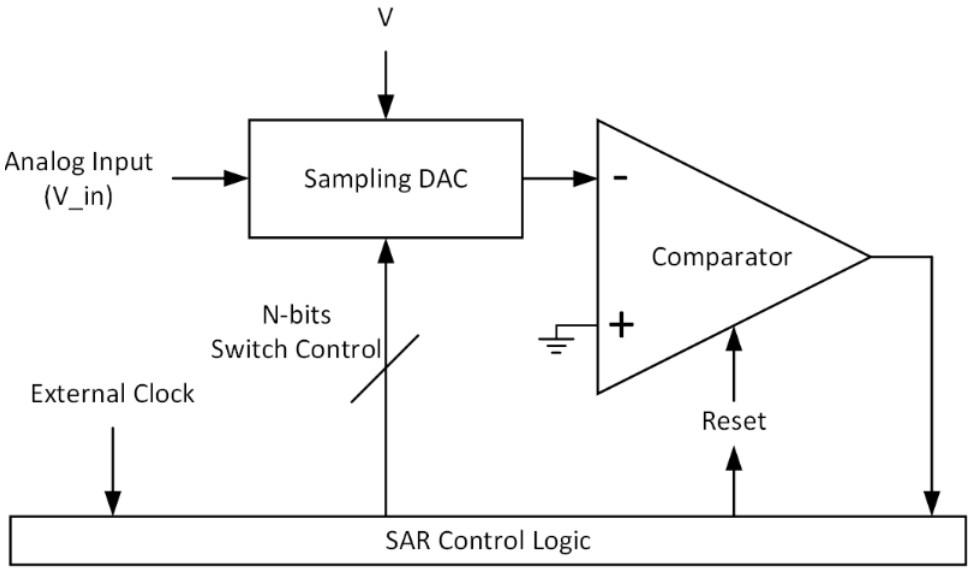

Figure 1. The structural principle of SAR ADC

SAR ADCs offer the following advantages: First of all, due to its simple structure, SAR ADC can operate without complex circuit designs, secondly, simple circuit lead to a faster speed for the whole ADC, to name but not least, the circuit does not have many kinds of Conversion type electronic components, which literally let SAR ADCs have a higher ENOB. However, its simple structure also brings some problems: all components must be ensured to operate normally, or it may come to a shutdown. Moreover, its principle of operation determines the operating time, so that when the demand for ENOB increases, it will cost a longer time [14]. Therefore, SAR ADC is always used in the condition of medium and low speeds and high-resolution requirements, such as industrial measurement and control and automotive electronics.

3.2. Flash ADC

Flash ADC is composed of a voltage divider resistor network, a blank of comparator and a priority encoder, which demonstrates in the figure 2. The resistor network is composed of 2N resistors, and divides voltage range of [0 to Vref] into 2N-1 segments. After the input of Vin, going through the comparator and generating 2N-1 digital codes, finally convert to the output by the priority encoder[15].

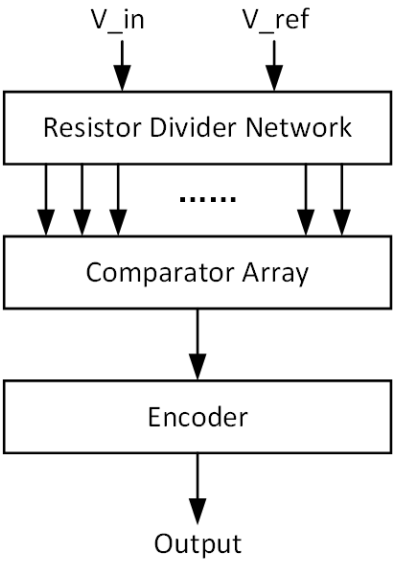

Figure 2. The operational principle of Flash ADC

Fast is the Flash ADC's advantage, due to its fully parallel of comparing process, all comparisons can be completed in one go. But its disadvantage, one is Flash ADC occupies a larger chip area and more energy consumption caused by it many requirements for different components. The higher the requirement for ENOB, the more complex the circuit will become. Another one is the models of all components have to match each other, or it will cause an error. So, the Flash ADC generally used in the field of high-speed communication.

3.3. Sigma-Delta ADC

The given figure 3 demonstrates how does the Sigma-Delta ADC work. It firstly oversampling the analog signal, putting the effective signal into a wider frequency, which literally decrease the interference of the noise sound. Then the ADC uses input signal X(n) and the feedback signal of DAC to make a subtraction, the result goes to the integrator, further reduce noise interference. Next, the signal is processed by a 1-bit comparator. By comparing the input voltage with a reference level (e.g. 0V), it performs a binary mapping to generate a 1-bit output Y(n), which only include 0 and 1. This data current will back to DAC part and compare with X(n), which formed a negative feedback system, led the final result more accurate. At last, after filtering and extraction, receive a high accuracy digital signal.

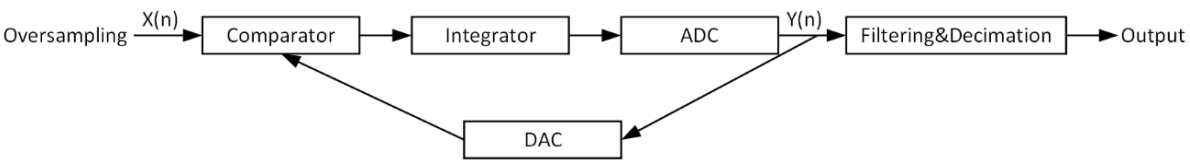

Figure 3. The operational principle of Sigma-Delta ADC

One of the distinctive advantages of Sigma-Delta ADC is it utilizes oversampling technique at the initial step, which can let resolution up to 16 to 24 bits, even higher. At the output part, digital filtering has filtered out a certain proportion of noise, which can better protect the original signal. These two designs effectively improve the anti-jamming capability of Sigma-Delta ADC. It is worth to mention that, although the accuracy of the output data is higher, this process needs more time to finish it, so Sigma-Delta ADC has a relatively low conversion speed

and a large delay. Therefore, Sigma-Delta ADC is mostly used in environments requiring high-precision and low-speed acquisition, such as medical equipment and audio applications.

3.4. Pipeline ADC

Pipeline ADC's entire conversion process is divided into several stages, each of them finish partial conversion tasks, and pass the residual signal to the next stage, different stages run in order, as the figure 4. Every stage is composed of ADC and DAC, the data from upper stage goes to the ADC of next stage, the result of upper stage will transfer to the redundant calibration module and its DAC part, which convert the residual signal back into an analog signal and pass it to the next stage, loop until the last level[16].

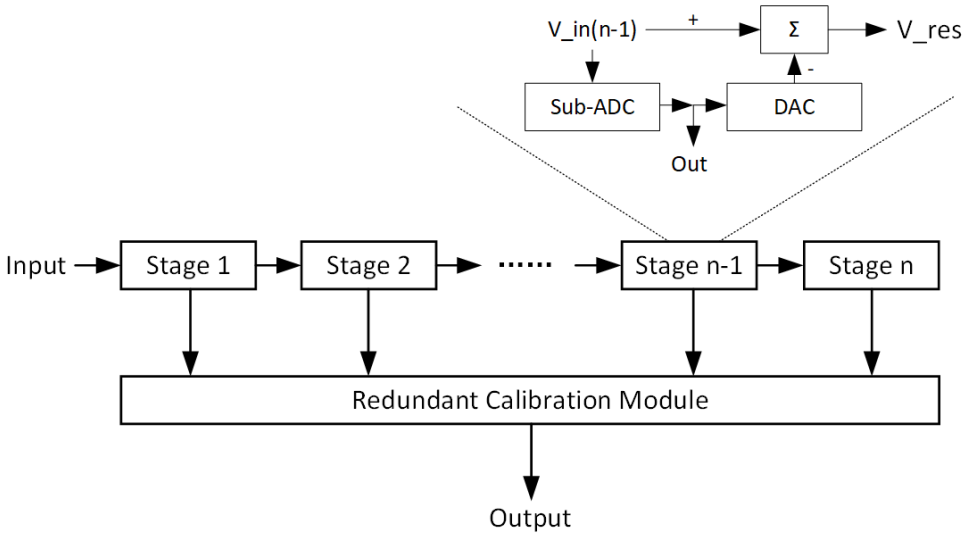

Figure 4. The structural principle of Pipeline ADC

Pipeline ADC is connected to many sub-circuits, which is structural simple and has a high scalability, dealing with lots of different data at the same time, which faster and a higher ENOB than SAR ADC. But it is the combination of many circuits that make the whole circuit more complex, moreover, there will be delays in hierarchical processing. Therefore, Pipeline ADC is used in normal communication, video and other fields.

4. Hybrid and Emerging Technologies

The above four ADCs all have their own advantages and disadvantages. By leveraging their respective strengths and compensating for their weaknesses, a superior performance can be achieved. So, their some new technology are worth to pay attention to.

4.1. Pipeline-SAR ADC

Just like what the name described, this ADC is the combination of Pipeline and SAR ADC, as a hybrid ADC. It retains the hierarchical form of the Pipeline ADC, but in each stage, the sub-ADC is changed to SAR ADC, which in the figure 3.5, the ADC part is replaced by SAR ADC. The whole operation principle is similar with the Pipeline ADC, respectively, the SAR ADC or the sub-ADC receive analog signals from the previous stage, convert them into digital signals, and transmit them to the DAC and the redundant calibration module, which is the digital logic module.

The sub-ADC of traditional Pipeline ADC uses Flash ADC. Although it is relatively fast, its drawbacks are very obvious that consumption and occupied area is large. It is using SAR ADC that have a lower speed than the traditional structure, which need to compare N times, but the consumption and the area of the ADC will slump immediately. It is a worthwhile exchange that

let Pipeline-SAR ADC show significant advantages in terms of power consumption, area and design complexity [17].

4.2. Flash-SAR ADC

The previous text described that the advantage of Flash ADC is its extremely fast processing speed, which parallel circuit is able to finish convert at once. However, caused by its high consumption and low accuracy, it is difficult for Flash ADC using in such high accuracy environment. The low power consumption and high precision of SAR ADC can just make up for this. Therefore, if combine two ADC together, letting them run in different step, as figure 5 demonstrates. Input the analog signal simultaneously into the Flash ADC and SAR ADC part, operating the primary conversion. Because of the low accuracy of Flash ADC, it just output the first few digit number to the digital module, and the SAR ADC which has a lower speed but more precise, the output also goes to the digital module. Finally, output the final result after the module integration. This kind of result not only faster than the SAR ADCs, but also more precise than the Flash ADCs, which fully combines the characteristics of two different ADCs [18].

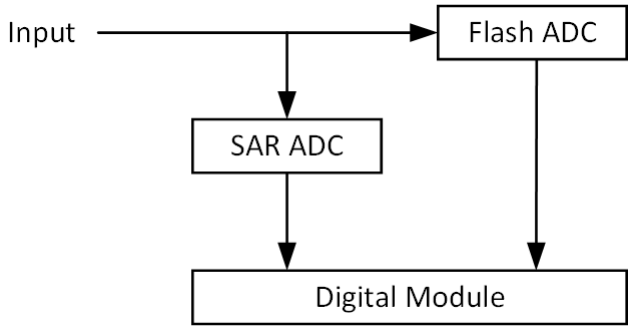

Figure 5. Flash-SAR ADC schematic diagram

4.3. Novel Hybrid ADC

All the ADCs mentioned above are of a fixed type and fixed structure, in the practical operation, some more different conditions are hard to avoid, those fixed structures may not absolutely meet the requirement. This is the reason why novel hybrid ADC comes out. For instance, in some situations, it might be necessary to split the aforementioned fixed-type ADC into smaller parts, which is useful for the requirement or put it into another system to generate a new type of ADC. It is also possible to modify or reorganize the components of a fixed type of ADC in different ways.

In recent years, Texas Instruments (TI) company has many new products in this field which are worth to pay attention to. The company continuously launch a series of high-performance ADC, the power consumption, sampling rate, noise signal and other aspects have been further optimized. Through functions such as integrated drivers, reference buffers and digital down-conversion, simplified the front-end signal chain design and reduced the overall system cost and size.

Table 1 can be concluded as four points. First of all, the sampling rate is positively correlated with power consumption, the ADC which has high sampling rate usually has a large power consumption, such as ADS9129, ADS9217 compare with ASD8695W, the power consumption of the first two with high sampling rates is both 360mW, and the latter one has a low sampling rate corresponds to low power consumption. Moreover, the high sampling rate and low consumption ADC ADS9326 is because its compact package and dual-channel optimization design. Secondly, the increase of ENOB may not have any influence with other factors, such as the SNR, ADS9212 is an 18 bits ADC, but it has similar SNR with the different model of ADC in

the table. Thirdly, most of new ADC adopt a dual-channel simultaneous sampling design, simplified the multi-sensor system, enhanced the system integration also controlled the changes of other factors such as consumption. And the last one is SAR ADC, which exhibits broad applicability among emerging ADC architectures. It may be its advantage of average performance and small area occupy, or the TI company is more mature in the technology of SAR ADC, adding some other functions on the basic SAR ADC, which lead to an increase of power consumption. To sum up, TI's new ADC achieves diverse designs by optimizing the SAR architecture and packaging.

Table 1. Recent New ADCs of TI Company

Device Model	Sampling Rate/ksps	Power Consumption/ mW	Signal-to-Noise Ratio/dB	Effective Number	Stucture
ADS9129	20000	360	94	16	SAR ADC with ADC Driver and Reference Driver
ADS8685W	500	42	80	16	SAR ADC
ADS9326	3000	40	93	16	Dual-Channel, Simultaneous-Sampling SAR ADC in a Compact Package
ADS9217	5000	360	95.1	18	Dual-Channel, Simultaneous-Sampling Input Driver for SAR ADC
ADS9815	1000	220	-	18	Dual-Channel Simultaneous Sampling ADC
ADS9212	8000	220	92.3	18	Dual-Channel Simultaneous Sampling ADC

5. Discussion

The development of ADCs should focus on these core areas: Firstly, utilize new architectures and advanced processes and materials to improve the performance of ADC, secondly, when it at various environments, it is adaptive ability that help ADCs to make appropriate adjustments, and the last one is combined with artificial intelligence (AI) and machine learning (ML) to have a performance breakthrough.

To meet the growing system requirements, the architecture design of ADC is shifting from single circuits to combination and is now becoming more diversiform. The single-architecture ADC mentioned above, such as SAR ADC which is suitable for high resolution conditions at normal speeds, their applicable scenarios include data acquisition for industrial control systems and sensors, and due to its low power consumption, it is also used in many portable electronic devices. The structure of Flash ADC allows it to have an extremely high sampling rate, which can maximize information acquisition and make it suitable for real-time signal processing. For the Pipeline ADC, benefit from their pipelined architecture, results in a fast conversion speed, but the power consumption is higher, therefore, it is suitable for applications such as communication and imaging. And oversampling type Sigma-Delta ADC, known for its high resolution and low noise, is suitable for applications where require high precision but relatively low demand for speed, such as high precision sensors. However, the rise of hybrid architectures has significantly enhanced overall performance. The Flash-SAR ADC mentioned above, which uses Flash ADC to perform coarse conversion at first, and then use SAR ADC to improve the accuracy, which is more precise than Flash ADC and faster than SAR ADC. This hybrid approach performs well in environments with high dynamic demands, allowing for real-

time adjustments to balance metrics such as resolution, conversion speed, and power consumption. This signifies that ADC architecture is evolving towards modular intelligence. It is worth to mention that the noise-shaping successive approximation ADC (NS-SAR ADC) is one of the most promising in the new structure dimension. It combines the high power efficient and precision characteristics of SAR ADC and Sigma-Delta ADC. The NS-SAR ADC embeds the SAR ADC into a noise shaping loop similar to the Sigma-Delta ADC, this loop uses negative feedback to push the noise signal generated by the SAR ADC to a higher frequency and high-frequency noise can be filtered out using digital filters, which can literally improve the SNR of ADC, furthermore, improving the ENOB. However, there are still challenges that have to overcome. One is that digital filters are mostly analog circuits, to filter high-frequency noise, they must ensure high linearity, or the filter itself will generate new errors. Secondly, higher-order noise shaping results in greater circuit complexity, but this does not diminish it is an futural available strategies.

In terms of manufactural process, it is rapidly evolving towards nanometer-scale nodes and high integration levels to reduce ADC size, lower power consumption, and improve performance. For instance, in the time-staggered SAR ADC design, it utilizes a 22nm fully depleted silicon-on-insulator (FD-SOI) process, effectively improve the sampling rate and linearity, lower power consumption[19]. Another example is InP DHBT process, it provides lower latency for high-speed transistors, allowing quantizers to operate at extremely fast rates, and have rapidly sampling in a higher frequency condition, reduce the limitations from front-end devices and enhance the overall bandwidth[20]. Or utilizing second- and third-generation semiconductors, such as gallium arsenide (GaAs), indium phosphide (InP), gallium nitride (GaN), and silicon carbide (SiC), these categories of semiconductors have a critical breakdown voltage ten times that of silicon and a thermal conductivity three times that of silicon, allowing them to withstand more extreme conditions, moreover, electrons drift much faster in semiconductors, allowing them to operate at higher frequencies[21]. However, these methods above are not the few ways to improve the performance of the ADC, meanwhile, heterogeneous integration technologies, such as through-silicon vias (TSV), fan-out wafer-level packaging (FOWLP), and 3D ICs, have become mainstream, driving the close integration of ADCs and digital circuits[22]. TSMC expects to begin mass production of its 2nm process in 2025 and further develop the 1.4nm node in 2027. These creative technologies will enhance the integration level of ADC a lot, effectively alleviates the problem of process mismatch between analog and digital circuits. It lays a solid foundation for the Chiplet multi-chip module architecture and is expected to significantly reduce the overall energy consumption of the system, expanding its application potential in more fields.

In practical application, the ADC begins to conduct deep matching with specific scenarios. In the field of intelligent driving, high-performance ADCs can effectively support LiDAR signal processing and the raw signal pipeline of radar, and provide high sampling rates and low-latency data conversion for real-time environment identification and accurate response[23]. About medical equipment, especially for the wearable sensors such as PPG/ECG SoC, using SAR ADC achieve static low power consumption, and also support high resolution acquisition of SpO2 and heart rate, which does not need frequent charging. Its dynamic range is as wide as 133dB, with tremendous quality factors[24]. Otherwise, in high-precision data acquisition systems, broadband precision ADC optimizes the signal chain for industrial process control through multi-channel multiplexing and low-noise design, solving problems under high channel density. These applications are driving the evolution of ADC towards multi-functionality and low latency and promoting the transformation from general to customized models. Facing all environments, a single model cannot fully meet their needs at the same time. This requires the ADC to be adaptive, that is, to sense changes in its operating environment, input signals or internal components, and dynamically adjust its architecture parameters to

achieve the best energy efficiency ratio. For example, adaptive power scaling allows the ADC to dynamically adjust its power consumption based on real-time conditions. When the input signal amplitude is small, it appropriately reduces the current to lower real-time power consumption. Or in the environments with different resolution requirements, automatically switching resolutions can also effectively reduce power consumption.

However, at the nanometer level or even smaller process nodes, the limitations of circuit characteristics request high demands on factors such as manufacturing processes, circuit conditions and temperature, leading to a rapid increase in the architecture design and manufacturing costs of further high precision ADC. For this problem, using algorithm and AI to real-time monitoring, feedback, correction and enhancement of ADC performance is a choice which is the future trend that break through the limitations of circuit characteristics. The first is real-time modeling and dynamic error compensation. Nowadays, existing ADC operate offline, which consumes time and makes error correction online impossible during operation. Digital assistances such as algorithms can make this process dynamic, which requires real-time monitoring of key components inside the ADC and the establishment of a dynamic error model. For example, the dynamic error of an ADC can be caused by sampling clock jitter, power supply voltage or temperature fluctuations. Using the techniques described above, the ADC's redundancy and data stream are utilized during operation to assess and correct errors, ensuring high linearity and a high SNR are maintained in most environments. Secondly, machine learning is introduced based on this, to make modeling and error compensation more intelligent. By utilizing the powerful fitting capabilities of neural networks and a suitable amount of training data, we can identify the complex mismatches and nonlinear mapping relationships within the ADC, and promptly identify and compensate for errors. Meanwhile, machine learning and deep learning algorithms are used to make the complex quantization process more intelligent, improving conversion efficiency and anti-interference capabilities. For example, AI systems can automate the tuning of filter and quantizer parameters in Sigma-Delta ADC by using genetic algorithms to optimize the noise transfer function, which greatly shortens the design cycle and improves noise performance[25]. Machine learning will also be used for adaptive optimization of ADC, dynamically and automatically adjusting their own parameters to cope with different operating environments or make up for their own shortcomings, which has driven the evolution of ADC from passive converters to intelligent nodes.

6. Conclusion

This article systematically and respectively reviews the basic working principles and key indicators of analog-to-digital converters (ADC), compares the circuit characteristics and suitable applications of four mainstream structures: SAR, Flash, Sigma-Delta and Pipeline ADC, and discusses the design advantages of hybrid architectures represented by Flash-SAR and Pipeline-SAR ADC. Research has found that while individual architectures each have their advantages in specific indicators, hybrid architectures demonstrate greater competitiveness when faced with the combined demands of modern electronic information systems for high speed, high precision and low power consumption. Analysis of TI company’s latest products further confirms that dual-channel synchronous sampling and highly integrated packaging have become the mainstream trend in the industry. This has significant theoretical and practical value for driving performance breakthroughs in wireless communication MIMO systems, medical wearable devices and autonomous driving radar sensors.

However, this study still has some limitations. The paper focuses on theoretical analysis and architectural comparisons based on existing literature and products, lacking detailed analysis and verification of individual circuits within a specific hybrid architecture, as well as the specific

process effects in their practical application. Regarding the aforementioned limitations, firstly, EDA tools can be used to model the hybrid architecture down to a certain scale and analyze its process data; secondly, it can be placed in a real environment to test the dynamic performance of the ADC, which the data is more reliable. The future development of ADC technology will no longer be limited to innovation in the architecture itself, it will move towards deep integration across levels. On the one hand, as manufacturing processes advance towards nanometer nodes such as 2nm, heterogeneous integration technology will solve the process mismatch problem between analog and digital circuits. On the other hand, the introduction of AI and ML will make ADC more intelligent, breaking through the physical limits of traditional analog circuits through dynamic error modeling and adaptive calibration, and realizing the leap from a single data conversion device to an intelligent signal processing node.

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